

# TPS5420EVM-175 SWIFT™ Regulator Evaluation Module

## Contents

|   |                                       |    |
|---|---------------------------------------|----|
| 1 | Introduction .....                    | 1  |
| 2 | Test Setup and Results .....          | 3  |
| 3 | Board Layout .....                    | 8  |
| 4 | Schematic and Bill of Materials ..... | 11 |

## List of Figures

|    |  |    |
|----|--|----|
| 1  | Measured Efficiency, TPS5420 .....               | 4  |
| 2  | Load Regulation .....                            | 4  |
| 3  | Line Regulation .....                            | 5  |
| 4  | Load Transient Response, TPS5420 .....           | 5  |
| 5  | Measured Loop Response, TPS5420, VIN = 25 V..... | 6  |
| 6  | Measured Output Voltage Ripple, TPS5420 .....    | 6  |
| 7  | Input Voltage Ripple, TPS5420 .....              | 7  |
| 8  | Power Up, VOUT Relative to VIN .....             | 7  |
| 9  | Start-Up Waveform, VOUT Relative to ENA .....    | 8  |
| 10 | Top-Side Layout .....                            | 9  |
| 11 | Bottom-Side Layout (Looking From Top Side) ..... | 10 |
| 12 | Top-Side Assembly .....                          | 11 |
| 13 | TPS5420EVM-175 Schematic.....                    | 12 |

## List of Tables

|   |  |    |
|---|--|----|
| 1 | Input Voltage and Output Current Summary.....          | 2  |
| 2 | TPS5420EVM-175 Performance Specification Summary ..... | 2  |
| 3 | Output Voltages Available .....                        | 3  |
| 4 | EVM Connectors and Test Points .....                   | 3  |
| 5 | TPS5420EVM-175 Bill of Materials .....                 | 13 |

## 1 Introduction

This user's guide contains background information for the TPS5420 as well as support documentation for the TPS5420EVM-175 evaluation module (HPA175). Also included are the performance specifications, the schematic, and the bill of materials for the TPS5420EVM-175.

### 1.1 Background

The TPS5420 dc/dc converter is designed to provide up to a 2-A continuous, 3-A peak output from an input voltage source of 5.5 V to 36 V. Rated input voltage and output current range for the evaluation module is given in [Table 1](#). This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS5420 regulator and does not reflect the high input voltages that may be used when designing with this part. The switching frequency is internally set at a nominal 500 kHz. The high-side MOSFET is incorporated inside the

SWIFT, PowerPAD are trademarks of Texas Instruments.

TPS5420 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS5420 to achieve high efficiencies and helps to keep the junction temperature low at high output currents. The compensation components are provided internal to the integrated circuit (IC), whereas an external divider allows for an adjustable output voltage. Additionally, the TPS5420 provides an enable input. The absolute maximum input voltage is 36 V.

**Table 1. Input Voltage and Output Current Summary**

| EVM            | INPUT VOLTAGE RANGE            | OUTPUT CURRENT RANGE |
|----------------|--------------------------------|----------------------|
| TPS5420EVM-175 | V <sub>IN</sub> = 10 V to 36 V | 0 A to 2 A           |

## 1.2 Performance Specification Summary

A summary of the TPS5420EVM-175 performance specifications is provided in [Table 2](#). Specifications are given for an input voltage of V<sub>IN</sub> = 12 V and an output voltage of 5 V, unless otherwise specified. The TPS5420EVM-175 is designed and tested for V<sub>IN</sub> = 10 V to 36 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. Maximum input voltage for the TPS5420EVM-175 is 36 V.

**Table 2. TPS5420EVM-175 Performance Specification Summary**

| SPECIFICATION            |                | TEST CONDITIONS   | MIN | TYP    | MAX | UNIT |
|--------------------------|----------------|---|-----|--------|-----|------|
| VIN voltage range        |                |   | 10  |        | 36  | V    |
| Output voltage set point |                |   |     | 5.0    |     | V    |
| Output current range     |                | V <sub>IN</sub> = 10 V to 36 V  | 0   |        | 2.5 | A    |
| Line regulation          |                | I <sub>O</sub> = 1 A, V <sub>IN</sub> = 3 V - 6 V                     |     | ±0.11% |     |      |
| Load regulation          |                | V <sub>IN</sub> = 25 V, I <sub>O</sub> = 0 A to 2.5 A                 |     | ±0.1%  |     |      |
| Load transient response  | Voltage change | I <sub>O</sub> = 0.75 A to 2.25 A                                     |     | -40    |     | mV   |
|                          | Recovery time  |   |     | 200    |     | μs   |
|                          | Voltage change | I <sub>O</sub> = 2.25 A to 0.75 A                                     |     | +40    |     | mV   |
|                          | Recovery time  |   |     | 200    |     | μs   |
| Loop bandwidth           |                | V <sub>IN</sub> = 25 V  |     | 25.0   |     | kHz  |
| Phase margin             |                | V <sub>IN</sub> = 25 V  |     | 55     |     | °    |
| Input ripple voltage     |                | I <sub>O</sub> = 3 A  |     | 275    | 300 | mVpp |
| Output ripple voltage    |                |   |     | 32     |     | mVpp |
| Output rise time         |                |   |     | 7      |     | ms   |
| Operating frequency      |                |   |     | 500    |     | kHz  |
| Maximum efficiency       |                | V <sub>IN</sub> = 10 V, V <sub>O</sub> = 5 V, I <sub>O</sub> = 0.75 A |     | 93.2%  |     |      |

## 1.3 Modifications

The TPS5420EVM-175 is designed to demonstrate the small size that can be attained when designing with the TPS5420. A few changes can be made to this module.

### 1.3.1 Output Voltage Set Point

To change the output voltage of the EVM, it is necessary to change the value of resistor R2. Changing the value of R2 can change the output voltage above 1.25 V. The value of R2 for a specific output voltage can be calculated using [Equation 1](#).

$$R2 = 10 \text{ k}\Omega \times \frac{1.221 \text{ V}}{V_O - 1.221 \text{ V}} \quad (1)$$

[Table 3](#) lists the R2 values for some common output voltages. Note that V<sub>IN</sub> must be in a range so that the minimum on-time is greater than 200 ns, and the maximum duty cycle is less than 87%. The values given in [Table 3](#) are standard values, not the exact value calculated using [Equation 1](#).

**Table 3. Output Voltages Available**

| Output Voltage (V) | R2 Value (k $\Omega$ ) |
|--------------------|------------------------|
| 1.8                | 21.5                   |
| 2.5                | 9.53                   |
| 3.3                | 5.90                   |
| 5                  | 3.24                   |

### 1.3.2 Input Voltage Range

The EVM is designed to operate from a 10-V to 36-V input voltage range. The TPS5420 is specified to operate over an input voltage range of 5.5 V to 36 V.

## 2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS5420EVM-175 evaluation module. The section also includes test results typical for the TPS5420EVM-175 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

### 2.1 Input / Output Connections

The TPS5420EVM-175 is provided with input/output connectors and test points as shown in [Table 4](#). A power supply capable of supplying 2 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J3 through a pair of 20 AWG wires. The maximum load current capability should be 2 A. Wire lengths should be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the VIN input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

**Table 4. EVM Connectors and Test Points**

| Reference Designator | Function  |
|----------------------|---|
| J1                   | VIN, 10 V to 36 V   |
| J2                   | OUT, 5 V at 2 A maximum   |
| JP1                  | 2-pin header for enable. Connect EN to ground to disable, open to enable.               |
| TP1                  | VIN test point at VIN connector   |
| TP2                  | GND test point at VIN   |
| TP3                  | Output voltage test point at OUT connector  |
| TP4                  | GND test point at OUT connector   |
| TP5                  | Test point between voltage divider network and R3. Used for loop response measurements. |
| TP6                  | PH test point   |

### 2.2 Efficiency

The TPS5420EVM-175 efficiency peaks at load current of about 0.75 A, and then decreases as the load current increases towards full load. [Figure 1](#) shows the efficiency for the TPS5420EVM-175 at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs.

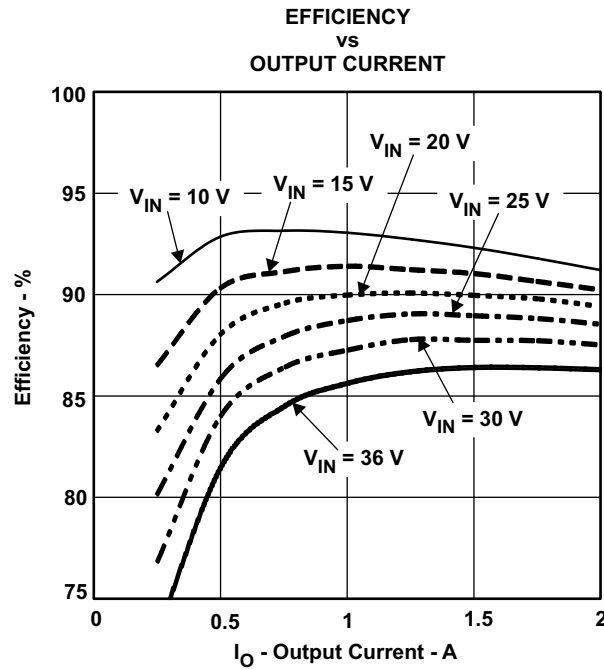


Figure 1. Measured Efficiency, TPS5420

### 2.3 Output Voltage Regulation

The output voltage load regulation of the TPS5420EVM-175 is shown in Figure 2; the output voltage line regulation is shown in Figure 3. Measurements are given for an ambient temperature of 25°C.

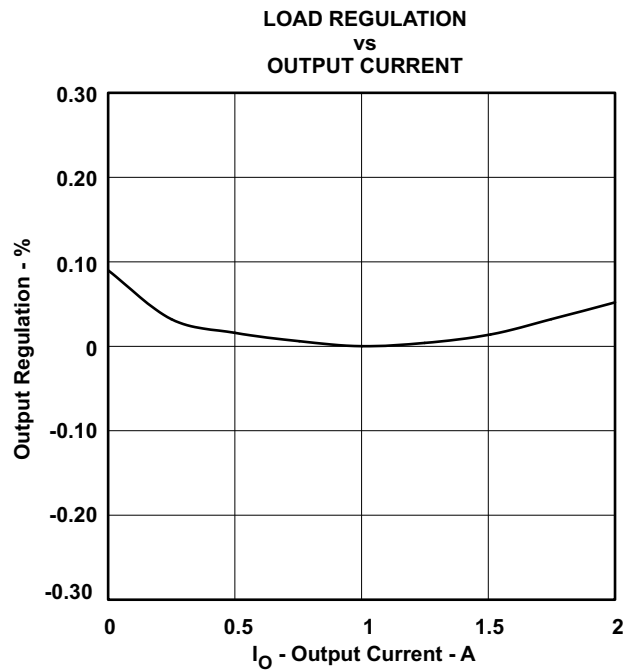


Figure 2. Load Regulation

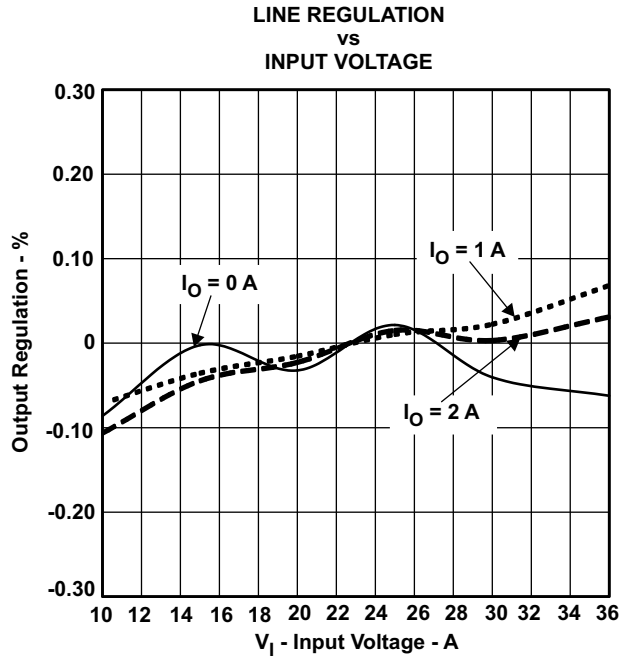


Figure 3. Line Regulation

## 2.4 Load Transients

The TPS5420EVM-175 response to load transients is shown in Figure 4. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

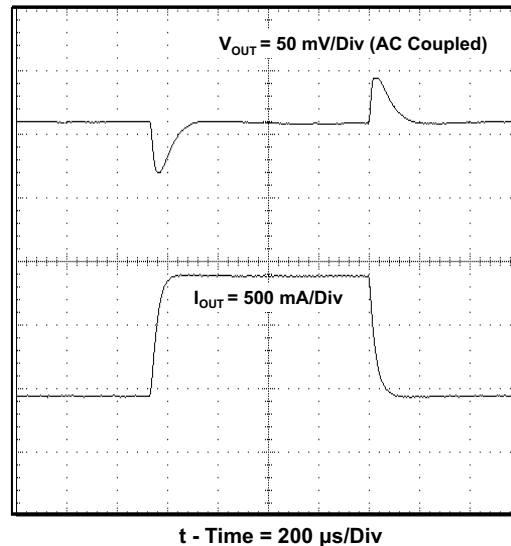


Figure 4. Load Transient Response, TPS5420

## 2.5 Loop Characteristics

The TPS5420EVM-175 loop-response characteristics are shown in [Figure 5](#) . Gain and phase plots are shown for VIN voltage of 25 V and a 1-A load current.

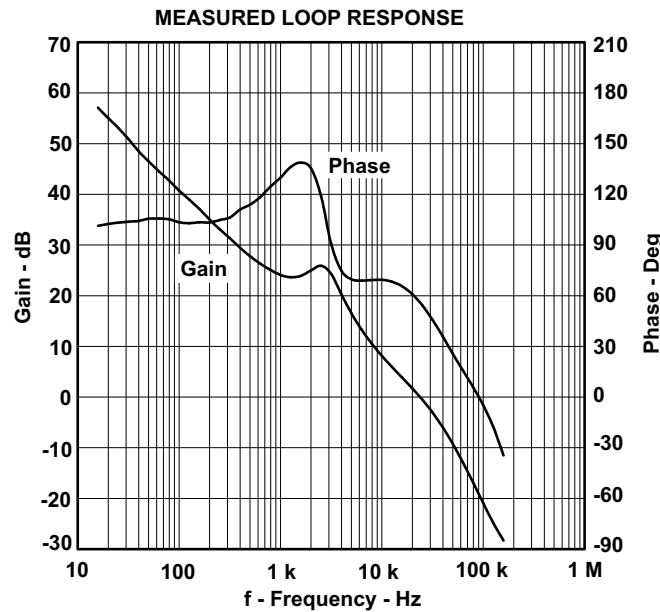


Figure 5. Measured Loop Response, TPS5420, VIN = 25 V

## 2.6 Output Voltage Ripple

The TPS5420EVM-175 output voltage ripple is shown in [Figure 6](#) . The input voltage is VIN = 25 V for the TPS5420. Output current is the rated full load of 2 A. Voltage is measured directly across output capacitors.

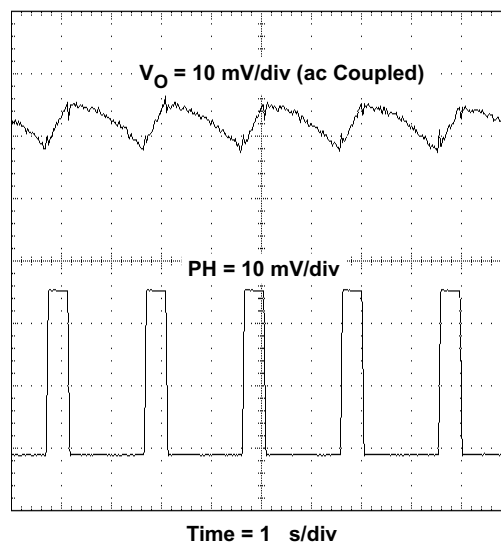


Figure 6. Measured Output Voltage Ripple, TPS5420

## 2.7 Input Voltage Ripple

The TPS5420EVM-175 input voltage ripple is shown in Figure 7. The input voltage is  $V_{IN} = 10\text{ V}$  for the TPS5420. Output current for each device is at full rated load of 2 A.

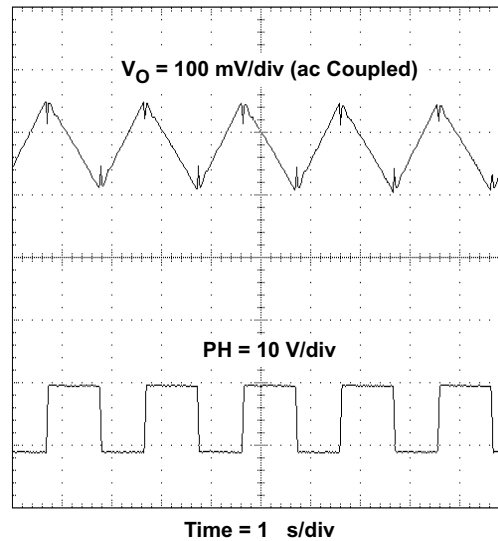


Figure 7. Input Voltage Ripple, TPS5420

## 2.8 Powering Up

The TPS5420EVM-175 start-up waveforms are shown in Figure 8 and Figure 9. In Figure 8 the top trace shows  $V_{IN}$  whereas the bottom trace shows  $V_{OUT}$ .  $V_{IN}$  increases from 0 V toward 25 V. When the input voltage reaches the internally set UVLO threshold voltage of 5.3 V, the slow-start sequence begins. The internal reference begins to ramp up linearly at the internally set slow-start rate towards 1.221 V, and the output ramps up toward the set voltage of 5 V. The output may be inhibited by using a jumper at JP1 to tie ENA to GND. When the jumper is removed, ENA is released and the slow-start sequence begins as shown in Figure 9. The top trace shows the ENA signal and the bottom trace shows  $V_{OUT}$ . When the ENA voltage reaches the enable-threshold voltage of 1.06 V, the start-up sequence begins as described above.

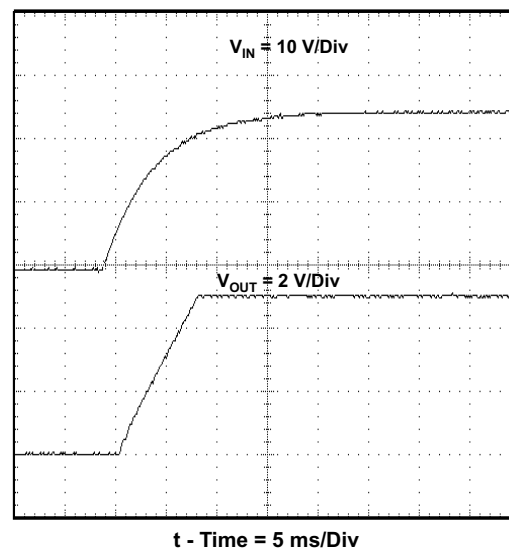
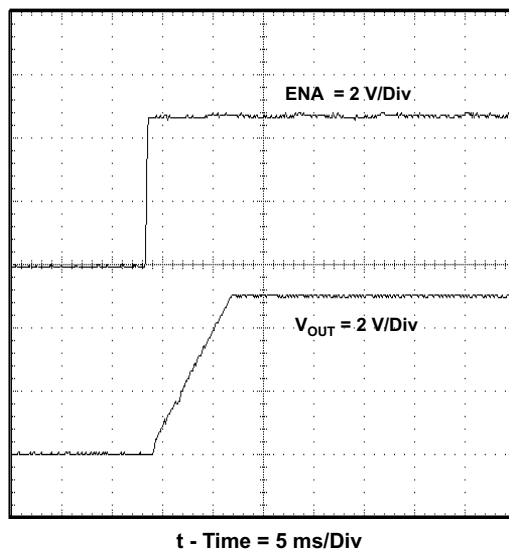


Figure 8. Power Up,  $V_{OUT}$  Relative to  $V_{IN}$



**Figure 9. Start-Up Waveform, V<sub>OUT</sub> Relative to ENA**

### 3 Board Layout

This section provides a description of the TPS5420EVM-175 board layout and layer illustrations.

#### 3.1 Layout

The board layout for the TPS5420EVM-175 is shown in [Figure 10](#) through [Figure 12](#). The top-side layer of the TPS5420EVM-175 is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for VIN, OUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS5420 and a large area filled with ground. The bottom layer contains ground and some signal routing. The top and bottom and internal ground traces are connected with multiple vias placed around the board including four vias directly under the TPS5420 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C1 and C4) and bootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, adjacent to the output capacitor C3.



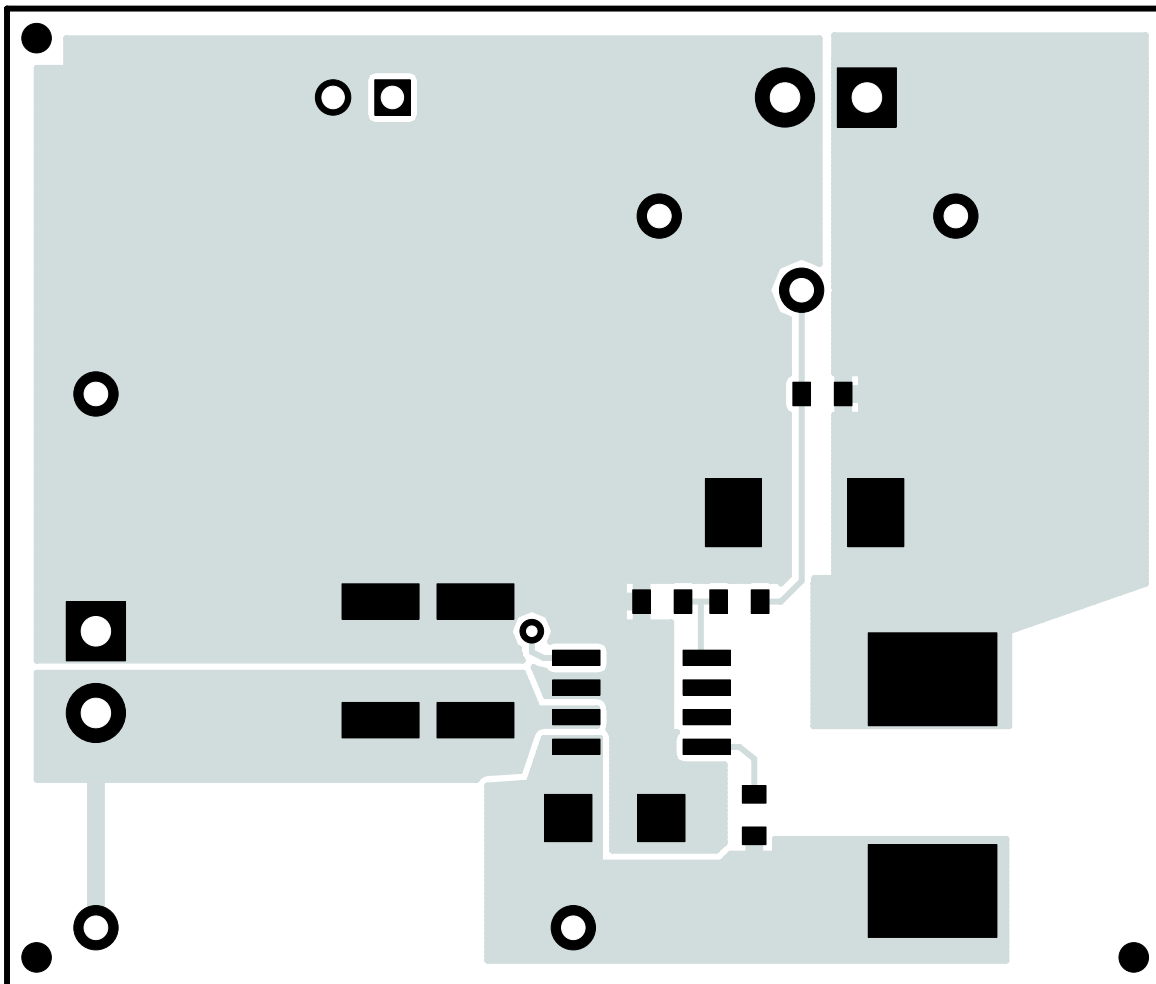


Figure 10. Top-Side Layout

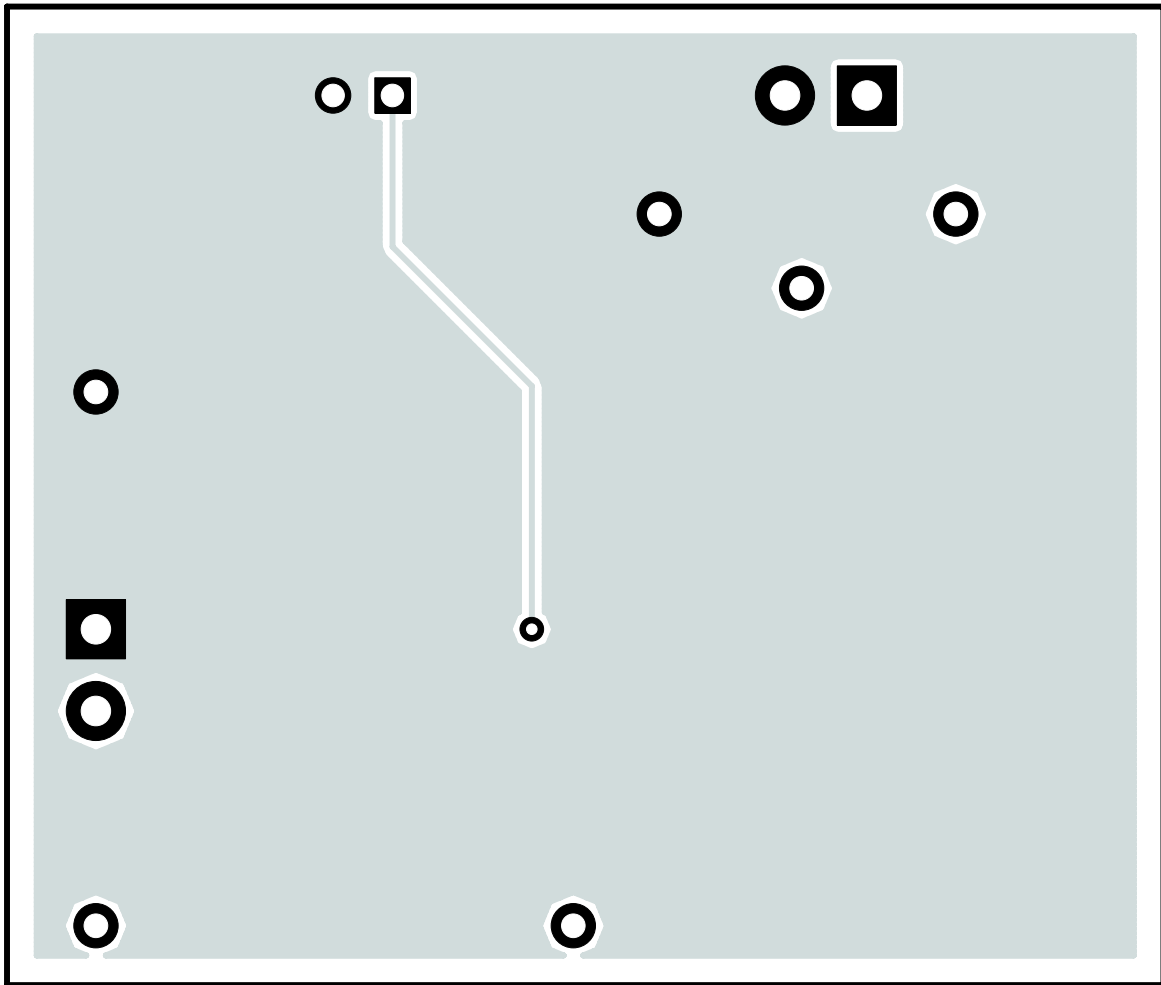


Figure 11. Bottom-Side Layout (Looking From Top Side)

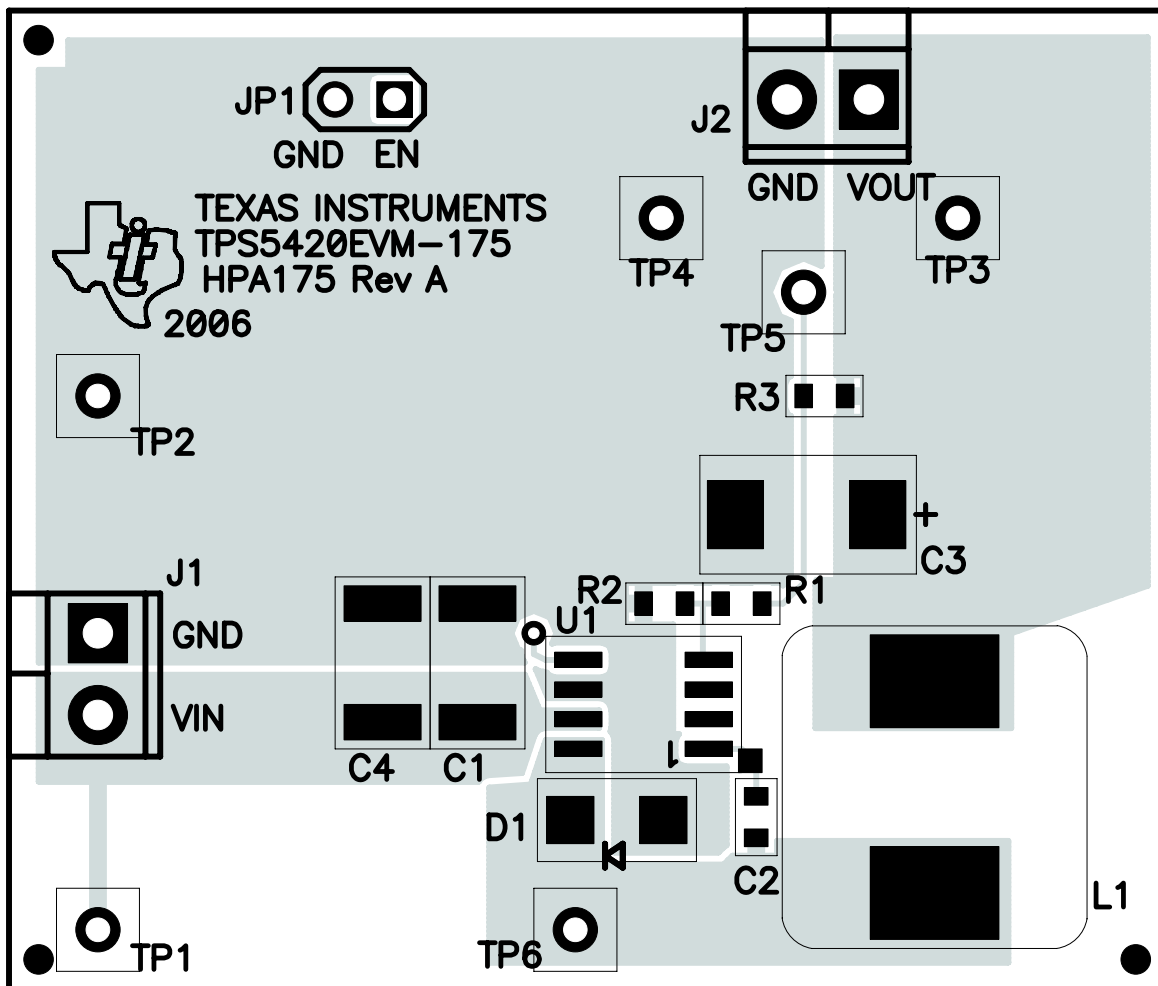


Figure 12. Top-Side Assembly

#### 4 Schematic and Bill of Materials

The TPS5420EVM-175 schematic and bill of materials are presented in this section.

### 4.1 Schematic

The schematic for the TPS5420EVM-175 is shown in [Figure 13](#).

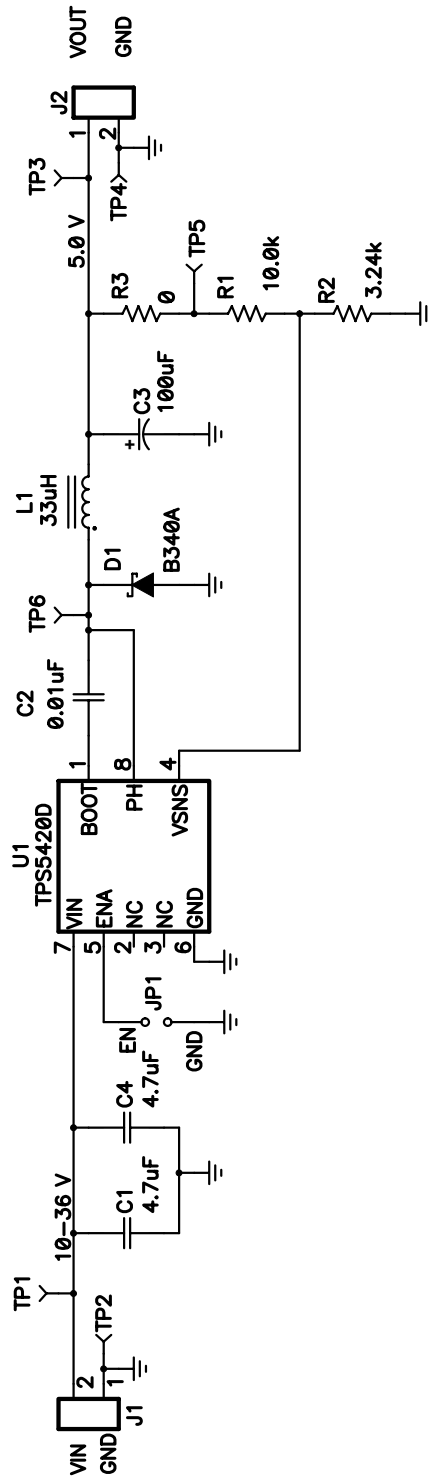


Figure 13. TPS5420EVM-175 Schematic

## 4.2 Bill of Materials

The bill of materials for the TPS5420EVM-175 is given by [Table 5](#).

**Table 5. TPS5420EVM-175 Bill of Materials**

| Count | REF DES               | Value        | Description                                   | Size          | Part Number      | MFR        |
|-------|-----------------------|--------------|---|---------------|------------------|------------|
| 2     | C1, C4                | 4.7 $\mu$ F  | Capacitor, Ceramic, 50V, X7R, 20%             | 1812          | C4532X5R1H475MT  | TDK        |
| 1     | C2                    | 0.01 $\mu$ F | Capacitor, Ceramic, 50V, X7R, 10%             | 0603          | C1608X7R1H103K   | TDK        |
| 1     | C3                    | 100 $\mu$ F  | Capacitor, Tantalum, 10V, 20%                 | 7343(D)       | TPSD107M010R0080 | AVX        |
| 1     | D1                    |              | Diode, Schottky, 3A, 40V                      | SMA           | B340A            | Diodes Inc |
| 2     | J1, J2                |              | Terminal Block, 2 pin, 6A, 3,5mm              | 0.27 x 0.25   | ED1514           | OST        |
| 1     | JP1                   |              | Header, 2-pin, 100mil spacing, (36-pin strip) | 0.100 x 2     | PTC36SAAN        | Sullins    |
| 1     | L1                    | 33 $\mu$ H   | Inductor, SMT, 2.2A, 75milliohm               | 0.484 x 0.484 | MSS1260-333      | Coilcraft  |
| 1     | R1                    | 10.0 k       | Resistor, Chip, 1/16W, 1%                     | 0603          | Std              | Std        |
| 1     | R2                    | 3.24 k       | Resistor, Chip, 1/16W, 1%                     | 0603          | Std              | Std        |
| 1     | R3                    | 0            | Resistor, Chip, 1/16W, 1%                     | 0603          | Std              | Std        |
| 4     | TP1, TP3,<br>TP5, TP6 |              | Test Point, Red, Thru Hole Color Keyed        | 0.100 x 0.100 | 5000             | Keystone   |
| 2     | TP2, TP4              |              | Test Point, Black, Thru Hole Color Keyed      | 0.100 x 0.100 | 5001             | Keystone   |
| 1     | U1                    |              | IC, Switching Step-Down Regulator, 36V, 2A    | SO8           | TPS5420D         | TI         |
| 1     | –                     |              | PCB, 1.95 In x 1.95 In x 0.062 In             |               | HPA175           | Any        |
| 1     | –                     |              | Shunt, 100-mil, Black                         | 0.100         | 929950-00        | 3M         |

## FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

## EVM TERMS AND CONDITIONS

Texas Instruments (TI) provides the enclosed Evaluation Module and related material (EVM) to you, the user, (you or user) **SUBJECT TO** the terms and conditions set forth below. By accepting and using the EVM, you are indicating that you have read, understand and agree to be bound by these terms and conditions. **IF YOU DO NOT AGREE TO BE BOUND BY THESE TERMS AND CONDITIONS, YOU MUST RETURN THE EVM AND NOT USE IT.**

This EVM is provided to you by TI and is intended for your **INTERNAL ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY**. It is provided "AS IS" and "WITH ALL FAULTS." It is not considered by TI to be fit for commercial use. As such, the EVM may be incomplete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product. As a prototype, the EVM does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this EVM not meet the specifications indicated in the EVM User's Guide, it may be returned within 30 days from the date of delivery for a full refund of any amount paid by user for the EVM, which user agrees shall be user's sole and exclusive remedy. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI TO USER, AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE OR NON-INFRINGEMENT.**

TI shall have no obligation to defend any claim arising from the EVM, including but not limited to claims that the EVM infringes third party intellectual property. Further, TI shall have no liability to user for any costs, losses or damages resulting from any such claims. User shall indemnify and hold TI harmless against any damages, liabilities or costs resulting from any claim, suit or proceeding arising from user's handling or use of the EVM, including but not limited to, (i) claims that the EVM infringes a third party's intellectual property, and (ii) claims arising from the user's use or handling of the EVM. TI shall have no responsibility to defend any such claim, suit or proceeding.

User assumes all responsibility and liability for proper and safe handling and use of the EVM and the evaluation of the EVM. TI shall have no liability for any costs, losses or damages resulting from the use or handling of the EVM. User acknowledges that the EVM may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the EVM it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

**EXCEPT TO THE EXTENT OF THE USER'S INDEMNITY OBLIGATIONS SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES WHETHER TI IS NOTIFIED OF THE POSSIBILITY OR NOT.**

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

User agrees to read the EVM User's Guide and, specifically, the EVM warnings and Restrictions notice in the EVM User's Guide prior to handling the EVM and the product. This notice contains important safety information about temperatures and voltages.

It is user's responsibility to ensure that persons handling the EVM and the product have electronics training and observe good laboratory practice standards.

By providing user with this EVM, product and services, TI is NOT granting user any license in any patent or other intellectual property right.

## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 10 V to 36 V and the output voltage range of 1.3 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

### **EVM WARNINGS AND RESTRICTIONS (continued)**

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2006, Texas Instruments Incorporated

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| <b>Products</b>  |  | <b>Applications</b> |  |
|------------------|--|---------------------|--|
| Amplifiers       | <a href="http://amplifier.ti.com">amplifier.ti.com</a>             | Audio               | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                   |
| Data Converters  | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>     | Automotive          | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>         |
| DSP              | <a href="http://dsp.ti.com">dsp.ti.com</a>                         | Broadband           | <a href="http://www.ti.com/broadband">www.ti.com/broadband</a>           |
| Interface        | <a href="http://interface.ti.com">interface.ti.com</a>             | Digital Control     | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Logic            | <a href="http://logic.ti.com">logic.ti.com</a>                     | Military            | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Power Mgmt       | <a href="http://power.ti.com">power.ti.com</a>                     | Optical Networking  | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
| Microcontrollers | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a> | Security            | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
|                  |  | Telephony           | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
|                  |  | Video & Imaging     | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
|                  |  | Wireless            | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated